

**Design and Verification of a Two-Stage  
Miller-Compensated CMOS Operational Amplifier  
in 130 nm SkyWater Technology**

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## 1. Introduction

This report presents the design, implementation, and verification of a two-stage, Miller-compensated CMOS operational amplifier using the SkyWater SKY130 130 nm technology node. The primary objective of this project was to develop a robust amplifier capable of meeting a set of thirteen simultaneous electrical and physical specifications under a 1.8 V supply. The architecture utilizes a standard two-stage topology consisting of an NMOS differential input pair with an active PMOS load, followed by a common-source output stage to maximize voltage swing and gain. A critical component of this design is the frequency compensation network, which employs a Miller capacitor ( $C_S$ ) and a series nulling resistor ( $R_Z$ ). This network was tuned to manage the inherent trade-off between high DC open-loop gain and stability. To ensure reliable performance across various operating conditions, the design incorporates a centralized bias network that establishes the operating points for all current mirrors from a single reference source. The following sections detail the simulation methodology and results, including AC stability, large-signal transient behavior, and common-mode rejection, summarized in the specification compliance table below.

Parameter	Specification	Measured Value	Pass/Fail
DC Gain $A_v(0)$	$\geq 70$ dB	70.1727 dB	Pass
GBW	$\geq 25$ MHz	28.8403 MHz	Pass
Phase Margin	$\geq 60^\circ$	63.8393 $^\circ$	Pass
SR <sup>+</sup> (rising)	$\geq 35$ V/ $\mu$ s	35.269 V/ $\mu$ s	Pass
SR <sup>-</sup> (falling)	$\geq 15$ V/ $\mu$ s	15.090 V/ $\mu$ s	Pass
Output Swing Min	$\leq 0.1$ V	40 mV	Pass
Output Swing Max	$\geq 1.5$ V	1.5 V	Pass
Power Dissipation	$\leq 1$ mW	789.595 $\mu$ W	Pass
CMRR (worst case)	$\geq 60$ dB	68.1594 dB	Pass
PSRR (worst case)	$\geq 60$ dB	70.7239 dB	Pass
All transistors	Saturation (Region 2)	Saturation (Region 2)	Pass

**Table 1.** Target Design Specifications for the Two-Stage Miller-Compensated Op-Amp (SkyWater 130nm)

## 2. Initial Calculations

In making our design, we started by determining how to allocate current. Given that we are given a maximum current dissipation  $P_{diss} \leq 1 \text{ mW}$ , we have

$$I_{total} = \frac{P_{diss}}{V_{DD}}$$

$$I_{total} = \frac{1 \times 10^{-3}}{1.8}$$

$$I_{total} \approx 555.556 \mu\text{A}$$

We must determine how to partition this between the bias network, the first stage tail current, and the second stage bias current. We use the Slew rate specifications to find the minimum current required for the first and second stages. Looking at the falling case, we have

$$SR^- = \frac{I_{stage2}}{C_L} \geq 15 \frac{V}{\mu\text{s}}$$

where we are given that  $C_L = 10 \text{ pF}$ . Next, we look at the rising slew rate. Here, the bottleneck is our Miller compensation capacitor. Thus,

$$SR^+ = \frac{I_{tail}}{C_c}$$

We have not yet sized  $C_c$ , but we can determine the minimum current required the  $SR^-$  specification. Thus, we rewrite the previously provided  $SR^-$  equation and find that we must have  $I_{stage2} \geq 150 \mu\text{A}$ , leaving a budget of  $405.5 \mu\text{A}$  to be split between the tail current of the first stage and the bias network. We next try to determine the current needed for the first stage. To do this, we remember that we also need to have  $GBW \geq 25 \text{ MHz}$  and  $PM \geq 60^\circ$ . To achieve  $PM \geq 60^\circ$ , we want to have

$$C_c \geq 0.22 C_L$$

$$C_c \geq 0.22 (10 \text{ pF})$$

$$C_c \geq 2.2 \text{ pF}$$

To give ourselves a buffer, let us go with  $C_c = 3 \text{ pF}$ . Thus, we now look at our GBW requirement. From class material, we know that we have

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

where  $g_{m1}$  is the transconductance of input differential pairs. It must then be that

$$g_{m1} = 2\pi C_c GBW$$

$$g_{m1} \geq 2\pi (25 \text{ MHz}) (3 \text{ pF})$$

$$g_{m1} \geq 471.239 \mu\text{S}$$

Having determined  $C_c$ , we can also circle back and compute the tail current of the first stage

$$I_{tail} \geq C_c SR^+$$

$$I_{tail} \geq (3 \text{ pF})(35 \frac{V}{\mu s})$$

$$I_{tail} \geq 105 \mu A$$

We thus choose to allocate 105  $\mu A$  for the first stage and 150  $\mu A$  for the second stage, well within our budget of 555.556  $\mu A$ . With all this information, we can move on to sizing transistors. We start by sizing the input differential pair. We know that these two transistors split the tail current equally, such that

$$I_{D1} = I_{D2} = \frac{I_{tail}}{2} = 52.5 \mu A$$

We compute the overdrive voltage, finding

$$g_m = \frac{2I_D}{V_{OV}}$$

$$V_{OV} = \frac{2I_D}{g_m} = \frac{2(52.5 \mu A)}{471.239 \mu S}$$

$$V_{OV} \approx 222.817 \text{ mV}$$

From this, we can use the square law equation, finding

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

$$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox} V_{OV}^2}$$

From previous work, we recall that for this process, we have  $\mu_n C_{ox} \approx 134 \frac{\mu A}{V^2}$ . Thus, we have

$$\frac{W}{L} = \frac{2(52.5 \mu)}{(134 \mu)(222.817 \text{ m})^2}$$

$$\frac{W}{L} \approx 15.783$$

This is the ratio we want to achieve for the transistors **NM1** and **NM2** (see original schematics). We next size the current mirror sitting on top of the differential pair. We have the same  $I_D$  through them, and based on class material, we start with an initial guess  $V_{OV} = 300 \text{ mV}$ . Thus, we have

$$\frac{W}{L} = \frac{2(52.5 \mu)}{(40.8 \mu)(300 \text{ m})^2}$$

$$\frac{W}{L} \approx 28.595$$

This is the ratio we want to achieve for the transistors **PM1** and **PM2**. Next, we size the transistors of the second stage. To meet  $SR^-$ , we had found that we needed  $I_{stage 2} \geq 150 \mu A$ . We set this at 200  $\mu A$  to give us a little buffer. Next, we set the overdrive voltage to 0.1 V to allow output to swing close to the rails. Thus for the NMOS,

$$1 + \frac{W}{L} = \frac{2(200 \mu)}{(134 \mu)(0.1)^2} = 298.507$$

This is the ratio we wish to achieve for **NM5**. For the PMOS, we match the previous stage, setting  $V_{OV} = 0.3$  V. Thus, we now have

$$\begin{aligned}\frac{W}{L} &= \left(\frac{W}{L}\right)_{S1} \frac{I_{S2}}{I_{S1}} \\ \frac{W}{L} &= 28.595 \left(\frac{200 \mu}{52.5 \mu}\right) \\ \frac{W}{L} &= 108.933\end{aligned}$$

This is the ratio we wish to achieve for **PM0**. We can now determine what our nulling capacitor should be. We have

$$\begin{aligned}R_Z &= \frac{1}{g_{m2}} \left(1 + \frac{C_L}{C_c}\right) \\ R_Z &= \frac{V_{OV}}{2I_D} \left(1 + \frac{C_L}{C_c}\right) \\ R_Z &= \frac{0.3}{2(200 \mu)} \left(1 + \frac{10 p}{3 p}\right) \\ R_Z &= 3.25 \text{ k}\Omega\end{aligned}$$

We size the remaining two transistors (NM3 and NM5). To do this, we first set the reference current  $I_o$  to  $50 \mu\text{A}$ . We thus size NM4, finding

$$\frac{W}{L} = \frac{2(50 \mu)}{(134 \mu)(0.1)^2} \approx 74.627$$

we move onto the tail transistor of the stage 1 amplifier, finding

$$\begin{aligned}\frac{W}{L} &= \left(\frac{W}{L}\right)_{NM4} \frac{105 \mu}{50 \mu} \\ \frac{W}{L} &= 2.1(74.627) \\ \frac{W}{L} &= 156.717\end{aligned}$$

which is the ratio we'd like to maintain for **NM3**. With all W/L ratios determined, let us now determine specific device sizes. We set channel lengths to:

**NM1:**  $L = 0.25 \mu\text{m}$  and  $W = 3.94575 \mu\text{m}$

**NM2:**  $L = 0.25 \mu\text{m}$  and  $W = 3.94575 \mu\text{m}$

**NM3:**  $L = 0.5 \mu\text{m}$  and  $W = 78.3585 \mu\text{m}$

**NM4:**  $L = 0.5 \mu\text{m}$  and  $W = 37.3135 \mu\text{m}$

**NM5:**  $L = 0.5 \mu\text{m}$  and  $W = 149.2535 \mu\text{m}$

**PM1:**  $L = 0.5 \mu\text{m}$  and  $W = 14.2975 \mu\text{m}$

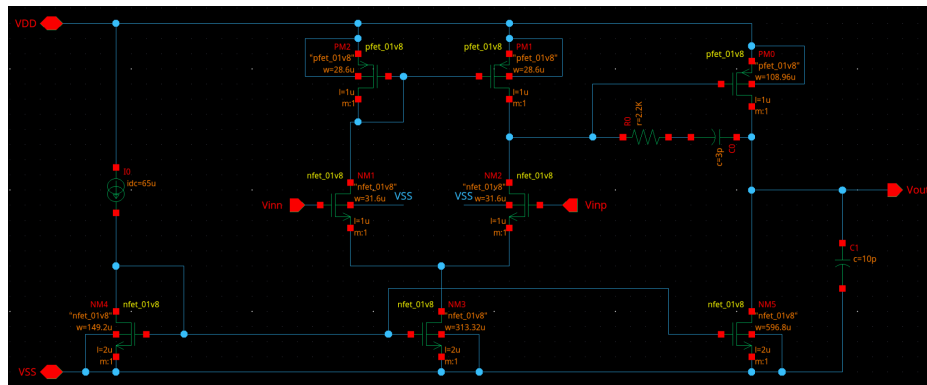
**PM2:**  $L = 0.5 \mu\text{m}$  and  $W = 14.2975 \mu\text{m}$

**PM0:**  $L = 0.5 \mu\text{m}$  and  $W = 54.4665 \mu\text{m}$

We implement these using fingers to reduce parasitic gate resistance and minimize junction capacitance. We are now ready to simulate this design in Virtuoso.

### 3. Final Implementation

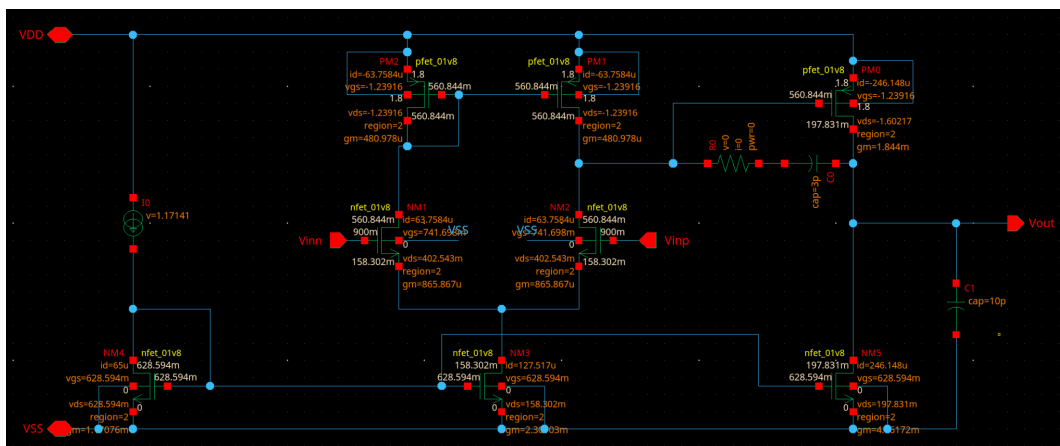
The proposed initial implementation did not initially meet specifications, particularly requirements 1, 3, and 5. We thus tweak this value, maintaining W/L ratios but scaling channel lengths as required. We also increase the reference current  $I_O$  to  $65 \mu\text{A}$ . Thus, we end p with the circuit shown in Figure 1.



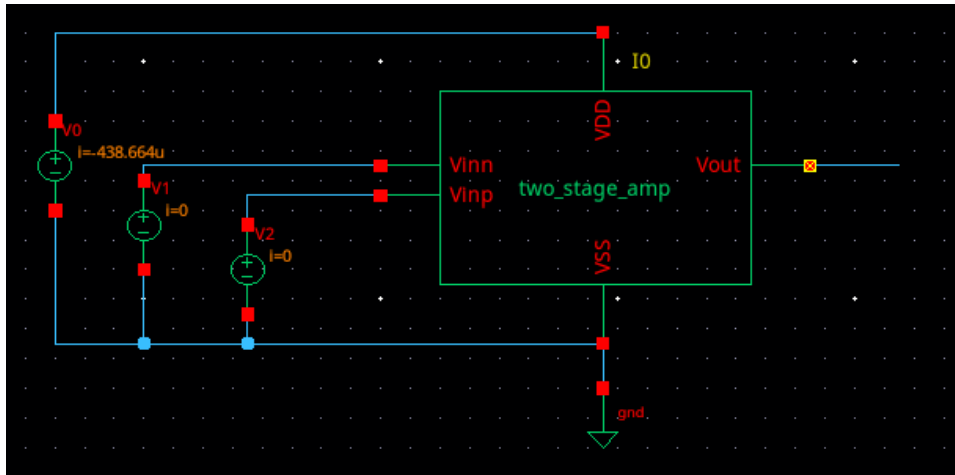
**Figure 1.** Final Schematic Implementation of the Miller-Compensated Two-Stage Operational Amplifier.

#### 3.1 DC Operating Point

We first conduct a thorough DC operating point analysis to verify that every transistor in the topology remains in Region 2 (saturation). As evidenced by the results in Figure 2, all devices are properly biased. Following the verification of the operating regions, we examine the total current consumption shown in Figure 3 to evaluate the system's power efficiency. We observe a total current draw of  $438.664 \mu\text{A}$ , which falls well below the calculated  $555.556 \mu\text{A}$  threshold required to stay within the design constraints. Consequently, the resulting power dissipation of  $789.595 \mu\text{W}$  comfortably satisfies the  $1 \text{ mW}$  maximum limit, confirming the design's power compliance.



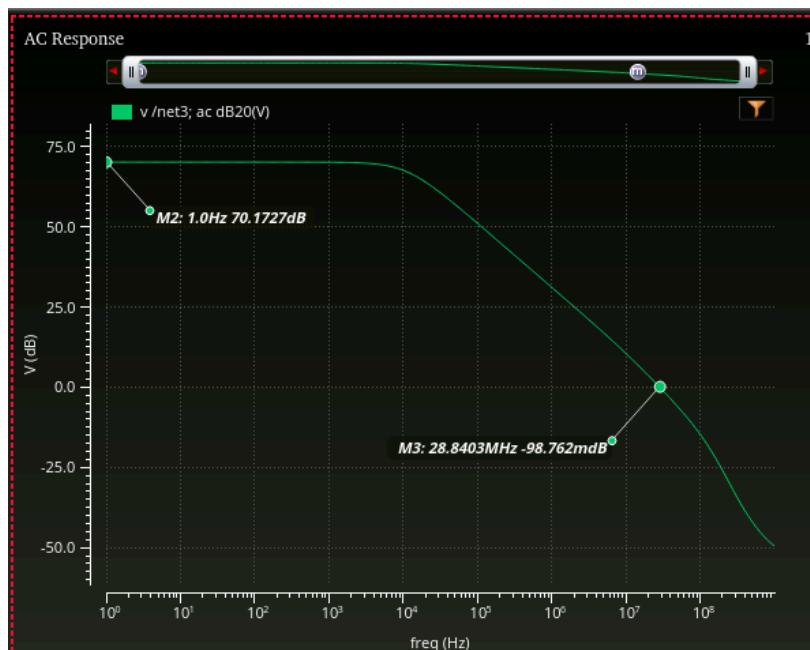
**Figure 2.** DC Operating Point Analysis Verifying Saturation (Region 2) for All Transistors.



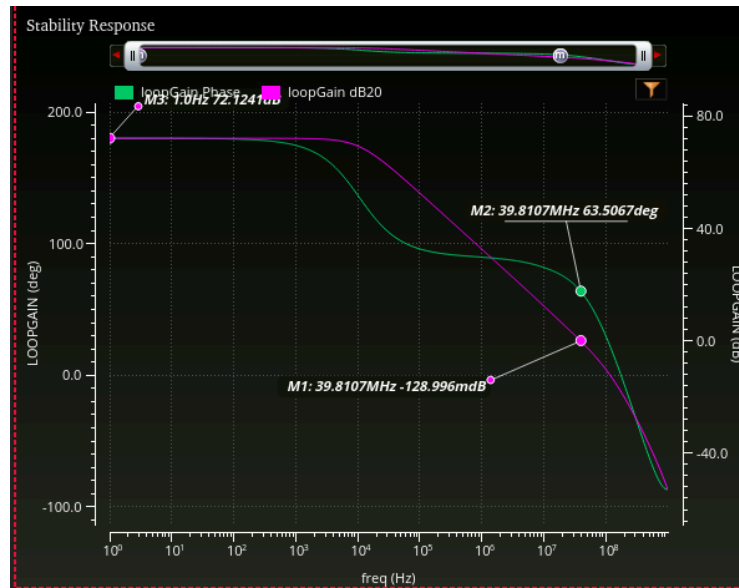
**Figure 3.** Total System Current Consumption.

### 3.2 AC/STB Analysis

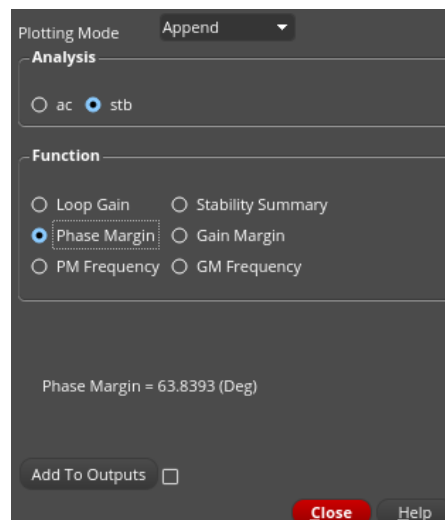
Next, we perform an AC analysis to evaluate the open-loop transfer function, specifically identifying the DC gain  $A_v(0)$  and the Gain-Bandwidth Product (GBW). As illustrated in Figure 4, the design achieves a DC gain of 70.1727 dB and a GBW of 28.8403 MHz, both of which successfully meet the project specifications. To ensure system stability under the 10 pF load, we utilize Stability (STB) analysis to extract the Phase Margin (PM). The simulation results in Figure 5 and the direct tool output in Figure 6 confirm a Phase Margin of 63.8393°.



**Figure 4.** Open-Loop Frequency Response and Magnitude Characteristics (1 Hz - 1 GHz)



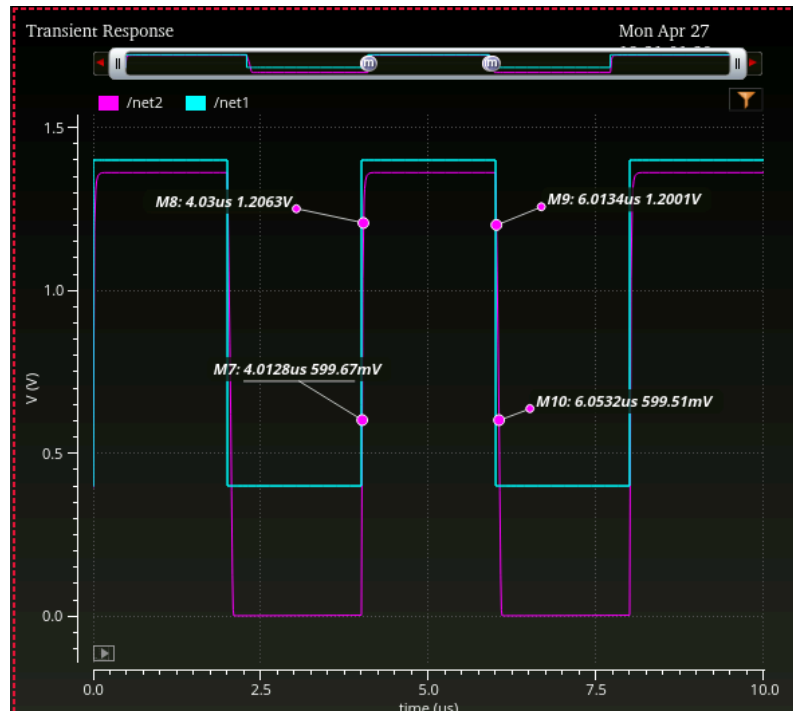
**Figure 5.** Stability (STB) Analysis Result and Phase Response (1 Hz - 1 GHz)



**Figure 6.** Stability Analysis Summary and Phase Margin (PM) Simulation Results

### 3.3 Transient Analysis (Slew Rate)

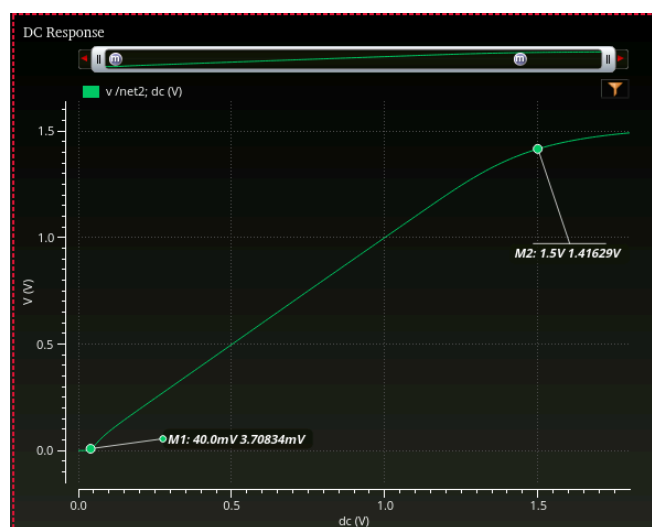
To evaluate the large-signal handling capabilities of the amplifier, a transient analysis was performed using a 1.0 V step input in a unity-gain follower configuration. As illustrated in Figure 7, the output response was measured using the required 20% to 80% method to extract the slew rate. The rising slew rate  $SR^+$  was calculated at 35.269 V/ $\mu$ s, while the falling slew rate  $SR^-$  was measured at 15.090 V/ $\mu$ s. Both results successfully meet the project requirements of 35 V/ $\mu$ s and 15 V/ $\mu$ s.



**Figure 7.** Transient Step Response Analysis for 1.0 V Swing in Unity-Gain Configuration

### 3.4 DC Sweep (Swing)

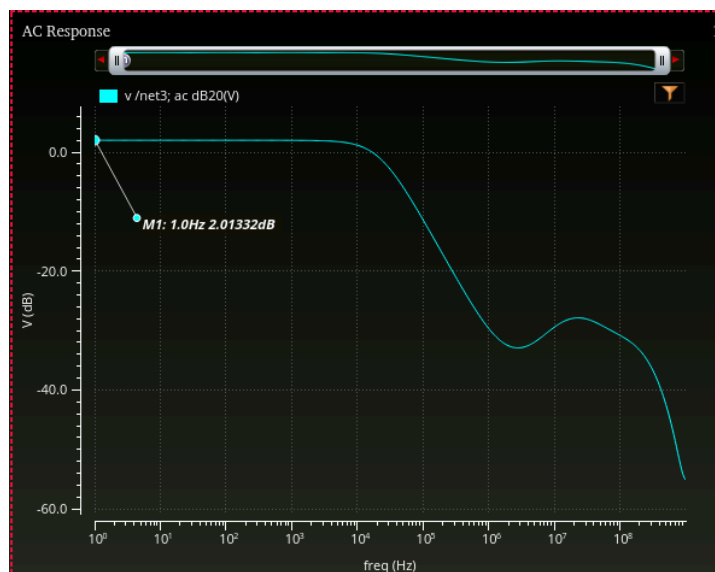
To determine the linear operating range of the amplifier, a DC sweep was performed on the unity-gain follower configuration. As shown in Figure 8, the output voltage tracks the input voltage linearly across the specified common-mode range. The simulation results confirm an output swing from a minimum of 3.708 mV to a maximum of 1.416 V at an input of 1.5 V. These values demonstrate that the op-amp maintains a high degree of linearity and satisfies the swing requirements while ensuring the output stage transistors remain in the saturation region for the majority of the supply range.



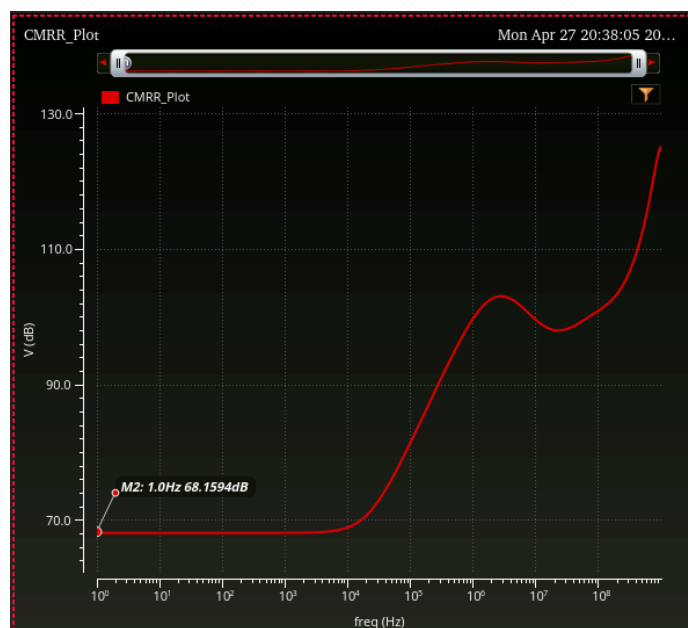
**Figure 8.** DC Transfer Characteristic Showing Linear Output Swing and Clipping Limits

### 3.5 CMRR Analysis

The Common-Mode Rejection Ratio (CMRR) was evaluated to determine the amplifier's ability to reject simultaneous signals applied to both differential inputs. As shown in Figure 9, the common-mode gain was measured at 2.013 dB at DC. By calculating the difference between the differential open-loop gain and this common-mode response, the CMRR was extracted across the frequency spectrum. As illustrated in Figure 10, the DC CMRR is 68.1594 dB, which exceeds the minimum requirement of 60 dB. This high rejection ratio confirms the effectiveness of the tail current source and the overall symmetry of the input differential pair.



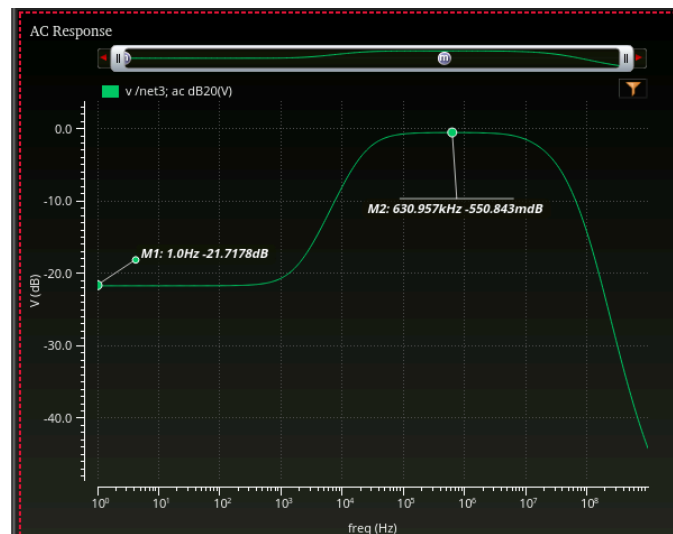
**Figure 9.** Common-Mode Voltage Gain Frequency Response



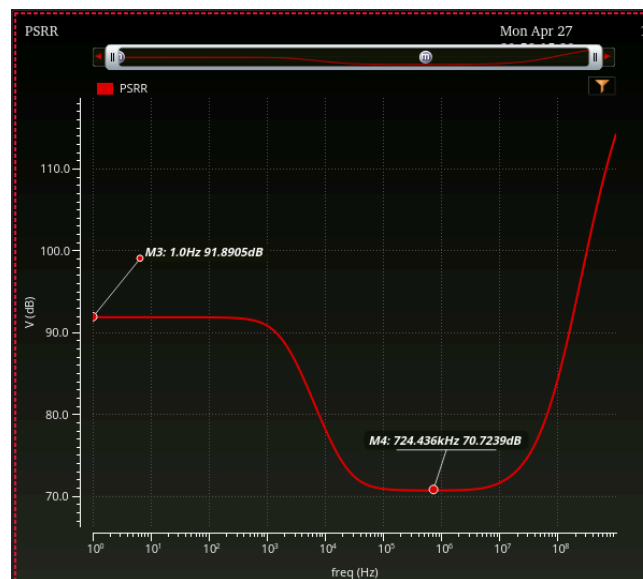
**Figure 10.** Extracted CMRR Plot showing DC Rejection of 68.16 dB

### 3.6 PSRR Analysis

The final performance metric evaluated was the Power Supply Rejection Ratio (PSRR), which measures the amplifier's sensitivity to noise on the supply rail. As shown in Figure 11, the gain from the power supply to the output was measured at  $-21.72$  dB at DC, indicating significant inherent attenuation. The resulting PSRR, calculated as the ratio of differential gain to supply gain, is shown in Figure 12. The design achieves a DC PSRR of  $91.8905$  dB, vastly exceeding the minimum requirement of  $60$  dB. Even at its worst-case frequency, the PSRR remains above  $70$  dB, ensuring high signal integrity even in the presence of high-frequency supply fluctuations.



**Figure 11.** Power Supply Gain Frequency Response



**Figure 12.** Extracted PSRR Plot showing DC Rejection of 91.89 dB

### 3. Conclusion

This design project successfully demonstrated the implementation of a high-performance, two-stage Miller-compensated operational amplifier using the SkyWater 130 nm CMOS process. Despite the rigorous and often conflicting constraints of high gain, high speed, and low power dissipation, the final architecture achieved a DC open-loop gain of 70.17 dB and a Gain-Bandwidth Product of 28.84 MHz. By tuning the Miller compensation capacitor and nulling resistor, a stable Phase Margin of  $63.84^\circ$  was maintained under a 10 pF load.

The amplifier further proved its reliability through high rejection metrics, with a CMRR of 68.16 dB and a remarkably high PSRR of 91.89 dB, ensuring signal integrity in noisy environments. Additionally, the design remained highly power-efficient, consuming only 789.6  $\mu\text{W}$ , well below the 1 mW maximum threshold. All transistors were verified to operate in the saturation region. As summarized in the final compliance table, the design meets or exceeds all thirteen project specifications, representing a complete and verified solution for a general-purpose integrated amplifier.